UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,893	10/02/2003	Robert C. Chang	SANDP040	2329

10027 7590 05/08/2006

ANDERSON, LEVINE & LINTEL L.L.P.
14785 PRESTON ROAD
SUITE 650
DALLAS, TX 75254

EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,893	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *2,12,22,29,35-37,39 and 43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-21,23-28,30-34,38,40-42,44 and 45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on April 18, 2006 regarding application 10,678,893 filed on October 2, 2003.

2. Claims 1, 3-8, 11, 13-18, 21, 23-26, 28, 30-34, 38, 40-42 and 44-45 have been amended.

Claims 2, 12, 22, 29, 35-37, 39 and 43 have been cancelled.

Claims 1, 3-11, 13-21, 23-28, 30-34, 38, 40-42 and 44-45 are pending under consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered, with Examiner's response set forth below.

Claims Previously Allowed, Now Rejected, New Art

The indicated allowability of claims 6, 16 26 and 33 in the previous Office Action are withdrawn in view of the newly discovered reference (Smith, US 6,961,890). A new ground of claim analysis based on Smith has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the

international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-7, 9, 11, 13-17, 19, 21, 23-26, 28, 30, 31-33, 35, 38, 40, 42 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith (US 6,961,890).

As to claim 1, Smith discloses **a method** [Dynamic Variable-Length Error Correction Code (title)] **for storing data within a non-volatile memory of a memory system** [data storage media such as silicon-based non-volatile memory are configured according to a data structure that segregates a payload portion and a redundancy portion (column 3, lines 16-18)] [figure 2], **the method comprising**: **identifying a first block into which the data is to be stored** [figure 2 shows a memory organization where data has been partitioned into a plurality of blocks (D0, D1, D2 and D3), any one of them may be considered as the first block];

obtaining an indicator associated with the first block, the indicator having a value indicative to the reliability of the first block [the corresponding indicator is the fundamental error rate; The quantity of resources devoted to redundancy is commonly based on the fundamental error rate of the data storage media. The fundamental error rate of a data storage media is the rate at which errors are found within the media. The fundamental error rate is dependent on a number of factors. For example, the technology type, media age, number of writes/reads and other factors can impact the fundamental error rate. Additionally, a composite memory device, such as a flash card formed from several integrated circuits, can have a complex error rate that reflects the distinct individual rates of each integrated circuit (column 1, lines 34-44); figures 3-4

show the error rate and the redundancy rate; note that the lower the error rate, the higher the reliability];

responsive to the indicator associated with the first block meeting a criterion [the criterion is a desired fundamental error rate], **encoding the data using a first error detection algorithm** [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36];

responsive to the indicator associated with the first block not meeting the criterion [the criterion is a desired fundamental error rate], **encoding the data using a second error detection algorithm** [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in

response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36], **the second error algorithm having a higher error detection capability than the first error detection algorithm** [Where necessary, the relative allocation of space between the payload and redundancy is dynamically adjusted. The space allocated to redundancy may then be associated with an appropriate ECC, selected from among an ECC library that may include parity, BCH (Bose-Chadhuri-Hocquenghem) codes and Reed-Solomon codes of varying strengths. Different ECC's have relative advantages and disadvantages in terms of the strength of their error detection and correction ability, their memory space requirements and the speed with which the executable program steps associated with the ECC execute (column 2, lines 43-53); thus the first error detection algorithm may be the parity, which has a lower error detection capability and the second algorithm may be the BCH codes, which has a higher error detection capability]; **and**

writing the data encoded using the first algorithm into the first block [figure 2 shows the encoded data, including the payload portion (D0, D1, D2, D3, ...) and the corresponding redundancy portion (E0, E1, E2, E3, ...)].

As to claim 3, Smith teaches that **the first algorithm is a 1-bit error correction code (ECC) algorithm** [For example, the payload portion may be an 8-bit data byte, and the redundancy may include one parity bit (column 3, lines 50-52)] **and the second algorithm is a 2-bit ECC algorithm** [Reed-Solomon codes of varying length, including 2-bit code (column 2, lines 43-53)].

As to claim 4, Smith teaches that **the indicator has a value indicative of whether the block is a reclaimed block** [In a typical application, the life cycle of the storage media results in some degradation over time. In response, error detection, recording and analysis are preformed. Media age and use levels are monitored (column 3, lines 38-41)].

As to claim 5, Smith teaches that **the indicator has a value indicative of a number of times the block has been erased** [In a typical application, the life cycle of the storage media results in some degradation over time. In response, error detection, recording and analysis are preformed. Media age and use levels are monitored (column 3, lines 38-41); For example, the technology type, media age, number of writes/reads and other factors can impact the fundamental error rate (column 1, lines 39-41)].

As to claim 6, refer to "As to claim 1." Further, Smith teaches that **the indicator has a value indicative of a number of times the block has been erased** [In a typical

application, the life cycle of the storage media results in some degradation over time. In response, error detection, recording and analysis are preformed. Media age and use levels are monitored (column 3, lines 38-41); For example, the technology type, media age, number of writes/reads and other factors can impact the fundamental error rate (column 1, lines 39-41)].

As to claim 7, Smith teaches that **the indicator has a value indicative of an approximately average number of times the blocks within the non-volatile memory has been erased** [In a typical application, the life cycle of the storage media results in some degradation over time. In response, error detection, recording and analysis are preformed. Media age and use levels are monitored (column 3, lines 38-41); For example, the technology type, media age, number of writes/reads and other factors can impact the fundamental error rate (column 1, lines 39-41)].

As to claim 9, Smith teaches that **the non-volatile memory is a flash memory** [a composite memory device, such as a flash card formed from several integrated circuits (column 1, lines 41-42)].

As to claim 11, refer to "As to claim 1." Further, it is understood in the art that the same error detection algorithm must be used for encoding and decoding to be able to recover the original data correctly.

As to claim 13, refer to "As to claim 3."

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

As to claim 16, refer to "As to claim 6."

As to claim 17, refer to "As to claim 7."

As to claim 19, refer to "As to claim 9."

As to claim 21, refer to "As to claim 1."

As to claim 23, refer to "As to claim 3."

As to claim 24, refer to "As to claim 4."

As to claim 25, refer to "As to claim 5."

As to claim 26, refer to "As to claim 6."

As to claim 28, refer to "As to claim 11."

As to claim 30, refer to "As to claim 3."

As to claim 31, refer to "As to claim 4."

As to claim 32, refer to "As to claim 5."

As to claim 33, refer to "As to claim 6."

As to claim 38, refer to "As to claim 1."

As to claim 40, refer to "As to claim 3."

As to claim 42, refer to "As to claim 11."

As to claim 44, refer to "As to claim 3."

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 13, 23, 30, 36, 40 and 44 are rejected under 35 U.S.C. 103(a) as being anticipated by Smith (US 6,961,890), and in view of Applicants' admission of prior art.

As to claims 3, 13, 23, 30, 36, 40 and 44, Smith teaches that **the first algorithm is a 1-bit error correction code (ECC) algorithm** [For example, the payload portion may be an 8-bit data byte, and the redundancy may include one parity bit (column 3, lines 50-52)] **and the second algorithm is a 2-bit ECC algorithm** [Reed-Solomon codes of varying length, including 2-bit code (column 2, lines 43-53)].

Further, Applicants admit in the "Background of the Invention" section of their disclosure that both the 1-bit and 2-bit ECC algorithms are well known in the art (paragraph 0009).

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that both the 1-bit and 2-bit ECC algorithms are well known in the art, as admitted by Applicants, hence lacking patentable significance.

8. Claims 9-10, 19-20, 27, 34, 37, 41 and 45 are rejected under 35 U.S.C. 103(a) as being anticipated by Smith (US 6,961,890), and in view of Kramer (US 6,182,239).

As to claims 9-10, 19-20, 27, 34, 37, 41 and 45, Smith does not mention that **the non-volatile memory is a flash memory, and particularly, one of a NAND flash memory and an MLC NAND flash memory.**

However, the invention of Smith is directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

9. Claims 4-5, 7-8, 14-15, 17-18, 24-25 and 31-32 are rejected under 35 U.S.C. 103(a) as being anticipated by Smith (US 6,961,890), and in view of Bruce et al. (US 5,956,743).

As to claims 4-5, 7-8, 14-15, 17-18, 24-25 and 31-32, Smith teaches that in a typical application, the life cycle of the storage media results in some degradation over time. In response, error detection, recording and analysis are preformed. Media age and use levels are monitored (column 3, lines 38-41); For example, the technology type, media age, number of writes/reads and other factors can impact the fundamental error rate (column 1, lines 39-41)

Further, Bruce et al. teach in their invention "Transparent Management at Host Interface of Flash-memory Overhead-Bytes Using Flash-Specific DMA Having Programmable Processor-Interrupt of High-Level Operations" a block management and replacement scheme for wear-leveling using ECC as part of the overhead bytes in a flash-memory chips [abstract] in which dual write counters are allocated to each of the

block to indicate how many times a block has been erased and written (i.e., reclaimed) [column 1, lines 57-67].

Using erase/write counters as indicators to support wear-leveling operations increases the life expectancy of a non-volatile memory device such as flash memory chip.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that benefit of using erase/write counters as indicators to support wear-leveling operation, as demonstrated Bruce et al., and to incorporate it into the existing scheme disclosed by Smith to further improve the life expectancy of the non-volatile memory devices.

As to claim 5, Bruce et al. teach that **the indicator is arranged to indicate a number of times the block has been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 7, Bruce et al. teach that **the indicator is arranged to indicate an approximately average number of times blocks within the non-volatile memory have been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 8, Bruce et al. teach that **the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator**

from the data structure [the data structure is the dual write counters that are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

As to claim 17, refer to "As to claim 7."

As to claim 18, refer to "As to claim 8."

As to claim 24, refer to "As to claim 4."

As to claim 25, refer to "As to claim 5."

As to claim 31, refer to "As to claim 4."

As to claim 32, refer to "As to claim 5."

10. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Blake et al., (US 5,228,046), "Fault Tolerant Computer memory Systems and Components Employing Dual Level error Correction and Detection with Disablement Feature."
- Bruce et al., (US 6,000,006), "Unified Re-Map and Cache-Index Table with Dual Write-Counters for Wear-Leveling of Non-Volatile Flash RAM Mass Storage."
- Stuart Fiske et al., (US 6,487,685), "system and Method for Minimizing Error Correction code Bits in Variable Sized Data Formats."

- Mokhlesi, (US Patent Application Publication 2004/0228197), "Compressed Event Counting Technique and Application to a Flash Memory System."
- Sukegawa et al., (US 5,603,001), "Semiconductor Disk System Having a Plurality of Flash memories."
- Takahashi, (US Patent Application Publication 2002/0008928), "Magnetic Disc Device and Error Correction Method Therefor."
- Bruce et al., (US 6,970,890), "Method and Apparatus for Data Recovery."
- Estakhri et al., (US Patent Application Publication 2001/0029564), "Identification and Verification of a Sector within a Block of Mass Storage Flash Memory."

Conclusion

11. Claims 1, 3-11, 13-21, 23-28, 30-34, 38, 40-42 and 44-45 are rejected as explained above.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

April 28, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
05/02/06